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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/765,931	01/19/2001	Vinodha Ramasamy	10005775-1	7462

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
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EXAMINER

VU, TUAN A

ART UNIT PAPER NUMBER

2124

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/765,931	Applicant(s) RAMASAMY ET AL.	
	Examiner Tuan A Vu	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 7/12/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 7/12/2004.

As indicated in Applicant's response, claims 1-3 have been amended; and claims 4-15 added. Claims 1-15 are pending in the office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eranian et al., "The Making of Linux / ia64", Internet Systems and Applications Laboratory, August 1999, pp. 1-11, <[url://www.hpl.hp.com/techreports/1999/HPL-1999-100.pdf](http://www.hpl.hp.com/techreports/1999/HPL-1999-100.pdf)> (hereinafter Eranian), in view of Gillies et al., USPubN: 2002/0083425 (hereinafter Gillies).

As per claim 1, Eranian discloses a method for allocating an N number of registers, comprising:

identifying a first statement allocating registers, the first statement is associated with a block of programming code (e.g. *function A*, Figure 5, pg. 3 – Note: allocating registers for a function implicitly discloses a block of related programming code);

identifying first parameters used in the first statement (e.g. *Inputs, Locals, Outputs*, r32...r52, Function A, Fig. 5); and

by using the number N and the first parameters as inputs, generating second parameters for use in a second statement (e.g. B: alloc r32=ar.pfs,5,4,0,0, r32...r41 – Fig. 5, pg. 3 – Note:

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reuse of *r32-r37* of statement A is using input of N number of registers and *r32-r41* amounts to second parameters being generated) to allocate the N number of registers.

But Eranian does not disclose that allocating N number of registers is for use in code instrumentation of the block of programming code. But Eranian discloses debug and simulation for porting purposes of the architecture of IA-64 kernel (e.g. *simulator, debugging*, pg. 4-7; *gdb* – pg. 9, left column), hence has suggested instrumentation of programming code, a concept so well known in the software development and code simulation and testing. Analogous to the modification of register input to provide increased output registers as by Eranian, Gillies discloses modification of the number of original registers are allowing additional registers to be available for code instrumentation (e.g. Fig. 2-4, 8-9). It would have been obvious for one of ordinary skill in the art at the time the invention was made to implement the register allocation techniques by Eranian so that it be used for code instrumentation as taught by Gillies because instrumenting with register modification instruction would dynamically enhance the register allocation for better accommodating to demand incurred during the process complex operations such as those susceptible to temporary storage, speculative execution or exception (see Gillies BACKGROUND).

As per claim 2, Eranian discloses first and second parameters including I registers, L registers and O registers (Fig. 5, pg. 3)

As per claim 3, Eranian disclose modifying O from the 1st parameters to yield O for the 2nd parameters (e.g. outputs from function A and combined output from B – Fig. 5, pg. 3)

As per claim 4, Eranian discloses second parameters comprise using N and O of the first input parameters in generating the O parameters for the second parameters (Fig. 5, pg.3 – Note:

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function A call *output parameters* r47-r52 matching with *Input parameters* r32-r36 of the Output of the B call is equivalent to using the O of the first parameters, while *r37-r41* in B output is the equivalent of N from the 1st parameters so that O from B is the combined O and N from the 1st parameters)

As per claim 5, Eranian discloses O of the 2nd parameters being N plus O from the first parameters (see Note of claim 4 above)

As per claim 6, this is a computer-readable medium version of method claim 1; hence is rejected using the corresponding rejections as set forth in claim 1.

As per claims 7-10, these claims correspond to claims 2-5 respectively; and are rejected with the corresponding rejection as set forth therein.

As per claim 11, this is a means plus function system version of method claim 1; hence is rejected using the corresponding rejections as set forth in claim 1.

As per claims 12-15, these claims correspond to claims 2-5 respectively; and are rejected with the corresponding rejection as set forth therein.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT

November 2, 2004


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